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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,344	08/28/2003	Sung-Yung Lee	5649-1162	6659

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,344	LEE ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-20* is/are allowed.

6)☐ Claim(s) *1-9,21-32 and 34* is/are rejected.

7)☒ Claim(s) *33 and 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed May 27, 2004 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because a copy of the figure(s) for this Korean publication was not included with the statement. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Claim Objections

2. Claims 29 and 31 are objected to because of the following informalities: the phrase "defines part of unit cell" is grammatically incorrect. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-9, 21-26, 28-32, and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Kashihara (USPN 6,458,284 B1).

5. In reference to claim 1, Kashihara (USPN 6,458,284 B1) discloses a similar device. Figure 12 of Kashihara discloses an interlayer dielectric (5) formed on a semiconductor substrate (13). A buried contact plug (4) extends a distance through the interlayer dielectric (5) to be in electrical communication with a predetermined region of the semiconductor substrate (13). An oxidation barrier pattern (3) is disposed on a top surface of the buried contact plug (4). A lower electrode (2) is disposed on the oxidation barrier pattern (3). A top surface area of the oxidation barrier pattern (3) is substantially equal to a bottom surface area of the lower electrode (2).

6. With regard to claim 2, the oxidation barrier pattern (3) comprises a metal nitride (column 1, lines 33-34).

7. In reference to claim 3, the lower electrode (2) of Kashihara meets the claim (column 1, lines 49-51).

8. With regard to claim 4, the external sidewalls of the lower electrode (2) and the oxidation barrier pattern (3) are aligned in a substantially straight line.

9. In reference to claim 5, an upper electrode (10) is disposed over the lower electrode (2). A dielectric film (9) is interposed between the lower electrode (2) and the upper electrode (10) thus forming a capacitor.

10. With regard to claim 6, the dielectric film (9) is made of BST or barium strontium titanate (column 1, lines 10-13). BST has a higher dielectric constant than ONO or oxide-nitride-oxide (see Huang, USPN 6,353,269 B1, column 6, lines 38-40), thus meeting the claim.

11. In reference to claim 7, the dielectric film (9) is made of BST or barium strontium titanate, a known ferroelectric substance (see Leung et al., USPN 5,563,762, column 1, lines 46-50), thus meeting the claim.

12. In reference to claim 8, the upper electrode (10) of Kashihara meets the claim (column 1, lines 49-51).

13. With regard to claim 9, figure 12 of Kashihara shows a transistor (18) which is connected to the oxidation barrier pattern (3) thus forming a memory cell.

14. In reference to claim 21, Kashihara (USPN 6,458,284 B1) discloses a similar capacitor. Figure 12 of Kashihara discloses an MIM capacitor with an upper electrode (10), a lower electrode (2), and a dielectric film (9) which is interposed between them. The lower electrode (2) has a bottom and a sidewall. The bottom of the lower electrode (2) is disposed over an oxidation barrier pattern (3) which defines a lower electrode platform with a top surface. The oxidation barrier pattern (3) resides above and is in electrical communication with a region of a semiconductor substrate (13). The bottom of the lower electrode

(2) has a surface area that is substantially coextensive with the surface area of the top surface area of the platform defined by the oxidation barrier pattern (3).

15. With regard to claim 22, the dielectric film (9) is made of BST or barium strontium titanate (column 1, lines 10-13). BST has a higher dielectric constant than ONO or oxide-nitride-oxide (see Huang, USPN 6,353,269 B1, column 6, lines 38-40), thus meeting the claim.

16. In reference to claim 23, the device of figure 12 resides in a unit cell of an integrated circuit DRAM memory device (column 1, lines 10-14).

17. In reference to claims 24 and 25, the device is in a unit cell of a DRAM memory device (column 1, lines 10-14). The dielectric film (9) of the unit cell is made of BST or barium strontium titanate, a known ferroelectric substance (see Leung et al., USPN 5,563,762, column 1, lines 46-50); thus forming a ferroelectric memory device.

18. In reference to claim 26, Kashihara (USPN 6,458,284 B1) discloses a similar semiconductor device. Figure 12 of Kashihara discloses a semiconductor device with a plurality of metal-insulator-metal capacitors. Each capacitor has an upper electrode (10), a lower electrode (2), and a dielectric film (9) which is interposed between them. The capacitors reside above a semiconductor substrate (13). Each capacitor has an oxidation barrier pattern (3) which is in electrical communication with respective regions of a semiconductor substrate (13). The lower electrode (2) of each capacitor has a bottom surface area which is substantially equal to the surface area of the upper surface of the underlying oxidation barrier pattern (3).

19. With regard to claim 28, the dielectric film (9) is made of BST or barium strontium titanate (column 1, lines 10-13). BST has a higher dielectric constant than ONO or oxide-nitride-oxide (see Huang, USPN 6,353,269 B1, column 6, lines 38-40), thus meeting the claim.

20. In reference to claim 29, the capacitor of figure 12 defines a part of a unit cell of an integrated circuit DRAM memory device (column 1, lines 10-14).

21. In reference to claims 30 and 31, the capacitor defines a part of a unit cell of a DRAM memory device (column 1, lines 10-14). The dielectric film (9) of the unit cell is made of BST or barium strontium titanate, a known ferroelectric substance (see Leung et al., USPN 5,563,762, column 1, lines 46-50); thus forming a ferroelectric memory unit cell.

22. With regard to claim 32, Kashihara (USPN 6,458,284 B1) discloses a similar fabrication method. Figure 12 of Kashihara discloses a plurality of MIM capacitors in unit cells of an integrated circuit memory device. An oxidation barrier pattern (3) is formed on a semiconductor substrate (13). A lower electrode (2) is disposed on the oxidation barrier pattern (3) so that a top surface area of the oxidation barrier pattern is substantially equal to a bottom surface are of the lower electrode (2).

23. In reference to claim 34, an interlayer dielectric layer (5) is formed on the semiconductor substrate (13) prior to forming the oxidation barrier pattern (3). A contact plug (40 is placed in the interlayer dielectric layer (5) so that it extends a distance through the interlayer dielectric layer (5) to be in electrical

communication with a predetermined region of the semiconductor substrate (13) prior to forming the oxidation barrier pattern (3).

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kashihara (USPN 6,458,284 B1).

26. With regard to claim 27, the lower electrode (2) of Kashihara in figure 12 has a closed continuous surface bottom. Kashihara teaches all of the claimed invention except for the cylindrical shape of the electrode. Although the Kashihara does not teach the exact cylindrical shape as that claimed by Applicant:

> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

Therefore claim 27 is not patentably distinguishable over the Kashihara reference.

Allowable Subject Matter

27. Claims 10-20 are allowed.

28. Claims 33 and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

29. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a fabrication method for a semiconductor device with a metal insulator metal capacitor containing a stack with a oxidation barrier pattern and a capping layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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